UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte THOMAS H. LEE, MARK G. JOHNSON,
CHRISTOPHER S. MOORE, ROGER W. MARCH,
and DANIEL T. BROWN

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Appeal No. 2005-2284
Application No. 09/748,589

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ON BRIEF

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Before KRASS, JERRY SMITH, and MACDONALD, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 126-141.

The invention pertains to a three-dimensional memory device with error checking and correction (ECC) circuitry, best

illustrated by reference to representative independent claim 126,

reproduced as follows:

126. A three-dimensional memory device with ECC circuitry comprising:

a support element;

error checking and correcting (ECC) circuitry carried by the support element; and

a memory array carried by the support element, wherein the memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another, wherein the memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers.

The examiner relies on the following references:

Hayashi	5,708,667	Jan. 13, 1998
Zhang	5,835,396	Nov. 10, 1998
Johnson et al. (Johnson)	6,034,882	Mar. 07, 2000
Leedy	6,208,545	Mar. 27, 2001
		(filed Nov. 17, 1997)
Anderson	6,321,358	Nov. 20, 2001
		(filed Aug. 27, 1998)

Claims 126-141 stands rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers either one of Zhang or Johnson, in view of Leedy, with regard to claims 126-135 and 138-141, adding to these combinations Hayashi, with regard to claim 136, and Anderson with regard to claim 137.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of obviousness under § 103, the examiner must produce a factual basis supported by a teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). The examiner may satisfy his/her burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to

combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With regard to the independent claims 126 and 130, the examiner contends that both Zhang (abstract, Figures 1, 4-6, column 1, lines 14-16, 63-67, column 2, lines 1-9, 16-26, and column 10, line 49 to column 11, line 28) and Johnson (abstract, Figures 4 and 5, column 1, lines 14-60, column 4, lines 11-22, column 12, lines 42 to column 13, line 25, column 16, lines 4-20, and column 18, lines 32-36) each individually teaches a three dimensional write-once memory device including a support element carrying a memory array comprising a plurality of cells arranged in a plurality of layers stacked vertically above one another, the memory cells deposited, patterned, and etched without using any bonding material between the layers. The examiner also points to Paper No. 35, at page 37, for an admission by appellants of these features being well known.

The examiner admits that neither Zhang nor Johnson discloses the ECC "circuitry carried by the support element" but contends that this arrangement is disclosed in the analogous 3-D array of Leedy (referring specifically to Leedy's Background section, Figure 2C, column 6, lines 61-66, and column 12, lines 23-31).

The examiner states that

> Clearly the ECC circuitry of Leedy is not specifically required for a 3-D memory with bonded layers, but rather as well known in the art allows for correction of errors which may become more prevalent in any higher density memory circuit, such as any 3-D memory. Thus it would have been obvious...to add ECC circuitry to the memories of Zhang and Johnson, because it was known to add this circuitry to the support element of high density 3-D memory arrays so that they could benefit from it's [sic, its] error correction capabilities (answer-page 4).

Appellants argue that Leedy fails to teach the recited memory array and that the skilled artisan would not have turned to either Zhang or Johnson to cure this deficiency, citing In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) for the proposition that a combination would not have been obvious within the meaning of 35 U.S.C. § 103 if the combination requires a substantial reconstruction and redesign of the elements in one of the references or a change in the basic principle under which the element in a reference was designed to operate (brief-page 6).

Applying Ratti to the instant case, appellants assert that since Leedy discloses a memory device that uses ECC and a stack of individual integrated circuits assembled after manufacturing and the primary focus of Leedy is the stacked integrated circuit memory, with ECC being merely an ancillary feature, in order to yield the instant claimed subject matter, Leedy's stack of

individual integrated circuits would be replaced with a monolithic structure in which memory cell layers are deposited, patterned, and etched without using any bonding material between the memory cell layers. This, argue appellants, would require transforming Leedy's post-manufacturing assembly process in which individual integrated circuits are stacked and bonded together to an "in situ" manufacturing process that forms a three-dimensional monolithic structure, and "such a modification would require a substantial reconstruction and redesign to Leedy's memory array and manufacturing process and, thereby, would change the basic operating principle disclosed in Leedy" (brief-page 7).

Additionally, appellants argue that Leedy "teaches away" from the examiner's proposed combination because Leedy distinguishes his stacked memory structure from a monolithic structure (brief-page 7).

We have reviewed the evidence before us, including the disclosures of the applied references and the arguments of appellants and the examiner, and we conclude from such a review that the examiner has presented a prima facie case of obviousness with regard to the subject matter of independent claims 126 and 130

and appellants' arguments have not convinced us of any error in the examiner's case.

Accordingly, we will sustain the rejection of claims 126 and 130 under 35 U.S.C. § 103.

The examiner has established a prima facie case of obviousness in showing that either one of Zhang or Johnson discloses the claimed subject matter but for the disclosure of the ECC "circuitry carried by the support element." Appellants do not dispute this. The examiner then offers Leedy to provide for the deficiency of the primary references, by showing that Leedy teaches ECC circuitry provided in a 3-D memory with bonded layers, allowing for correction of errors which may become more prevalent in any higher density memory circuit, such as any 3-D memory. The examiner then, quite reasonably in our view, concludes that it would have been obvious to add ECC circuitry to the memory of Zhang or Johnson, because it was known to add this circuitry to the support element of high density 3-D memory arrays so that they could benefit from error correction capabilities.

Yet, while the examiner's case is built on the modification of either one of the primary references (each showing the basic

structure of the claimed invention but for the ECC circuitry carried by a support element) by Leedy, appellants' major argument against the rejection focuses on an alleged impropriety of modifying Leedy by either one of the primary reference disclosures. Thus, appellants' arguments are not commensurate with the rejection set forth by the examiner and, as such, we find this line of argument unconvincing of nonobviousness of the instant claimed subject matter.

There is a big difference between the examiner's rejection rationale, modifying the three-dimensional memories of Zhang and Johnson to include ECC circuitry on a support element, based on a teaching of a third reference indicating that there is an advantage to having the capability to error check and correct, as proposed by the examiner, and the rejection apparently perceived by appellants wherein the teaching of ECC circuitry on a support element is somehow modified to include a memory array structure and method recited in claims 126 and 130.

At footnote 2 on page 7 of the brief, appellants finally come around to arguing the rejection as set forth by the examiner, in arguing that it would not have been obvious to add ECC circuitry to the memory arrays of Zhang and Johnson in order to benefit from error-correction capabilities because "ECC circuitry adds delays

and increases chip size, which is often undesirable in high-density memories that try to maximize the ratio of number of memory cells/chip size." Appellants conclude that the skilled artisan "would have followed conventional wisdom and **not** have added ECC circuitry to the memory arrays disclosed in Zhang and Johnson."

We disagree. As rightly pointed out by the examiner in response (answer-page 8), any such alleged disadvantages "were obviously not enough to prevent Leedy from incorporating it for their [sic, his] three dimensional high-density memory to achieve the well known aforementioned benefit of error correction capabilities." Thus, since Leedy appears to do what appellants assert the skilled artisan would not do (i.e., add ECC circuitry to memory arrays), in order to prevail, appellants would need to point to additional evidence as to why the artisan would not have taken the teachings of Leedy and applied them to the memory arrays of Zhang and/or Johnson.

As for appellants' "teaching away" argument, a reference may be said to "teach away" when a person of ordinary skill, upon [examining] the reference, would be discouraged from following the path set out in the reference or would be led in a direction divergent from the path that was taken by the applicant. In re Gurley, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994).

In the instant case, the fact that Leedy may teach the use of ECC circuitry in a stacked memory structure would not, in and of itself, dissuade artisans from employing such ECC circuitry in the memories disclosed by Zhang and/or Johnson and appellants have offered no evidence that it would.

Thus, we will sustain the examiner's rejection of claims 126-134, the claims indicated by appellants as constituting Group I, under 35 U.S.C. § 103.

Turning to the claims of Group II, i.e., claims 135 and 139-141, the examiner rejects these claims on the same grounds as the rejection of claims 126-134.

In addition to relying on the arguments, supra, with regard to non-combinability of the references, appellants specifically argue that Figure 2c of Leedy teaches the use of ECC circuitry in a memory controller circuit **in the memory device - not in a data storage system**, as required by independent claim 135, noting that neither Zhang nor Johnson teaches any type of ECC functionality, much less ECC functionality in a data storage system (see page 8 of the brief). Appellants argue further that there is no suggestion in the applied references to move the ECC circuitry from the memory device to the data storage system, specifically pointing to column

6, lines 61-64, of Leedy, indicating that the ECC circuitry is among components that are conventionally part of a memory device. It is appellants' position that the artisan "would no sooner move the ECC circuitry from the memory device to the data storage system as he would move the address decoders or listed components to the data storage system" (brief-page 9).

Claim 135 calls for a "data storage system" and "a memory device" which are coupled to the data storage system (we note, as did the examiner, that appellants do not appear to argue the "releasably" coupled aspect of the claimed invention). The claim further indicates that the data storage system comprises error checking and correcting (ECC) functionality.

Even though the claim has two separately labeled elements, "data storage system" and "memory device," it is true, as the examiner indicates at page 9 of the answer, that a "data storage system necessarily includes storage" and a memory device is part of a data storage system. Therefore, as the examiner states, ECC circuitry in the memory device is also in the data storage system. Since Leedy teaches ECC circuitry in a memory device, then it, broadly, also teaches the use of ECC circuitry in a "data storage system," as claimed.

Moreover, we endorse the examiner's view, at page 10 of the answer, that

> ...the general teaching of using ECC with a three-dimensional memory taught by Leedy would have been just as easily been implemented by an artisan with the ECC functionality off of the memory device, since that was the conventional implementation of ECC...even with the ECC circuitry on the memory device, the data storage system coupled thereto requires "ECC functionality" to the extent claimed to properly utilize and process the corrected data.

Appellants do not respond.

Accordingly, since the examiner's position appears reasonable to us and we have nothing from appellants convincing us otherwise, we will sustain the rejection of claims 135 and 139-141, constituting the Group II claims, under 35 U.S.C. § 103.

With regard to Group III, i.e., claim 136, this claim recites that the ECC functionality is implemented in software in the data storage system. The examiner relies on Hayashi for such a teaching (Figure 1, column 3, line 11 to column 4, line 13l; column 7, lines 37-39) and contends that it would have been obvious to implement the ECC functionality in the Zhang/Johnson/Leedy combination in software in the data storage system "because this is well known and provides the system adaptability and updatability" (answer-page 6).

Appellants agree that Hayashi teaches implementing ECC functionality in software, but contend that it does not teach implementing the ECC functionality in software "**in a data storage system**" (brief-page 9).

We, again, agree with the examiner. As explained by the examiner, at pages 10-11 of the answer, "since the memory device and its controller may be considered part of the data storage system, the ECC is implemented in software in the data storage system; however, even if the memory device is interpreted as separate from the data storage system, the controller or CPU is part of the data storage system (and thus also the software, and the ECC functionality)."

The examiner's explanation appears reasonable to us and we find nothing from appellants to convince us otherwise.

Accordingly, we will also sustain the rejection of claim 136, Group III, under 35 U.S.C. § 103.

With regard to Group IV, claim 137, this claim requires that the ECC functionality "is implemented in a file system in the data storage system." The examiner relies on Anderson, specifically Figure 31, column 22, line 64 to column 23, line 10 and column 24,

lines 37-52, for this limitation, contending that it would have been obvious to implement the ECC generator as part of the file system "because this would make of the device of the prior art combination useable with known file systems which incorporate ECC generation" [sic] (answer-page 6).

Appellants argue that Figure 31 of Anderson illustrate how file system information **is combined with, or embedded in,** ECC information prior to recording the information on the disc. Therefore, argue appellants, "it is clear that the file system information and the ECC information are separately generated" (brief-page 10) since the file system information is combined with or embedded in ECC information. Appellants conclude therefrom that the ECC functionality is not implemented in a file system, as required by claim 137.

Claim 137 does not require the ECC information and the file information to be generated simultaneously. Therefore, appellants' argument that the ECC information and the file information in Anderson are, somehow, generated separately, is not persuasive. As pointed out by the examiner, at page 11 of the answer, "the claim merely states that ECC is implemented in a file system, it is noted that the ECC of Anderson is used to reconstruct file system

information and thus is implemented in the file system to the extent claimed."

Appellants offer no explanation as to why the claim language should not, or could not, be so broadly interpreted. Accordingly, we will sustain the rejection of claim 137 (Group IV) under 35 U.S.C. § 103.

Finally, as to claim 138 (Group V), this claim recites that the ECC functionality is implemented in hardware in the data storage system. The examiner included this claim in the rejection under 35 U.S.C. § 103 based on the combination of either Zhang or Johnson, in view of Leedy, since it was understood that the ECC functionality of Leedy was implemented in hardware in the data storage system, as explained at pages 9-10 of the answer.

Appellants offer no rationale to rebut the examiner's seemingly reasonable conclusion, arguing, simply, that it is not only the ECC functionality implemented in hardware that is required but that it is implemented in hardware **in a data storage system** (brief-page 10).

We agree with the examiner for the reasons supra, anent claim 135. Therefore, we will sustain the rejection of claim 138 (Group V) under 35 U.S.C. § 103.

Since we have sustained each and every one of the examiner's rejections of claims 126-141 under 35 U.S.C. § 103, the examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
ALLEN R. MACDONALD Administrative Patent Judge	)

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